IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A semiconductor integrated circuit device includes a series connected TC unit type ferroelectric RAM which includes series connected memory cells each having a transistor having a source terminal and a drain terminal and a ferroelectric capacitor inbetween the two terminals, the device comprising:

first and second bit lines;

first and second plate lines;

a first series connected TC unit type structure which includes series connected memory cells, and has one terminal connected to the first bit line via a first selection transistor and the other terminal connected to the first plate line;

a second series connected TC unit type structure which includes series connected memory cells, and has one terminal connected to the second bit line via a second selection transistor and the other terminal connected to the second plate line;

word lines connected to gates of the series connected memory cells included in the first series connected TC unit type structure and gates of the series connected memory cells included in the second series connected TC unit type structure;

a plate line potential control circuit which controls, in a standby state, potentials of the first and second plate lines to a first potential and, in an active state, the potential of the first plate line from the first potential to a second potential and the potential of the second plate line from the first potential to a third potential when one of the series connected memory cells included in the first series connected TC unit type structure is selected; and

a bit line potential control circuit which controls a potential of the second bit line to the third potential, after charges are transferred from one of the ferroelectric capacitor included in the first series connected TC unit type structure to the first bit line.

Claim 2 (Original): The device according to claim 1, wherein the plate line potential control circuit controls the potential of the first plate line from the second potential to the third potential, after controlled to the second potential.

Claim 3 (Original): The device according to claim 1, wherein plate lines except the first and second plate lines maintain the first potential in the active state.

Claim 4 (Original): The device according to claim 1, wherein the bit line potential control circuit controls a potential of the first bit line to the third potential, after charges are transferred from one of the ferroelectric capacitor included in the first series connected TC unit type structure to the first bit line.

Claim 5 (Original): The device according to claim 1, further comprising:

an amplifier which uses the charges transferred to the first bit line as a signal and the second bit line as a complementary bit line, and amplifies the signal.

Claim 6 (Original): The device according to claim 5, further comprising:

a switch which electrically disconnects the amplifier from the first and second bit lines.

Claim 7 (Original): The device according to claim 6, wherein the switch electrically disconnects the amplifier from the second bit line when the potential of the second bit line is controlled to the third potential.

Claim 8 (Original): The device according to claim 6, wherein the switch electrically disconnects the amplifier from the first and second bit lines when the potential of the second bit line is controlled to the third potential.

Claim 9 (Currently Amended): The device according to claim 5, further comprising:

a third bit line; and

a fourth bit line, wherein the amplifier is shared among the first and second bit lines and third and fourth bit lines ~~different from the first and second bit lines~~.

Claim 10 (Original): The device according to claim 9, wherein the third and fourth bit lines are arranged in a memory cell array different from a memory cell array in which the first and second bit lines are arranged.

Claim 11 (Original): The device according to claim 10, wherein the first and third bit lines are electrically connected to one terminal of the amplifier, and the second and fourth bit lines are electrically connected to the other terminal of the amplifier.

Claim 12 (Original): The device according to claim 11, further comprising;

a switch which electrically connects and disconnects the amplifier from the first, second, third and fourth bit lines.

Claim 13 (Original): The device according to claim 12, wherein the switch electrically disconnects the second bit line from the amplifier and electrically connects the fourth bit line to the amplifier after charges are transferred from one of the ferroelectric capacitor included in the first series connected TC unit type structure to the first bit line.

Claim 14 (Original): An operation method for a semiconductor integrated circuit device includes a series connected TC unit type ferroelectric RAM which includes series connected memory cells each having a transistor having a source terminal and a drain terminal and a ferroelectric capacitor inbetween the two terminals, the device comprises,

first and second bit lines,

first and second plate lines,

a first series connected TC unit type structure which includes series connected memory cells, and has one terminal connected to the first bit line via a first selection transistor and the other terminal connected to the first plate line,

a second series connected TC unit type structure which includes series connected memory cells, and has one terminal connected to the second bit line via a second selection transistor and the other terminal connected to the second plate line, and

word lines connected to gates of the series connected memory cells included in the first series connected TC unit type structure and gates of the series connected memory cells included in the second series connected TC unit type structure, the operation method comprising:

controlling, in a standby state, potentials of the first and second plate lines to a first potential;

controlling, in an active state, the potential of the first plate line from the first potential to a second potential and the potential of the second plate line from the first potential to a third potential when one of the series connected memory cells included in the first series connected TC unit type structure is selected; and

controlling a potential of the second bit line to the third potential, after charges are transferred from one of the ferroelectric capacitor included in the first series connected TC unit type structure to the first bit line.

Claim 15 (Original): The operation method according to claim 14, wherein the potential of the first plate line is controlled from the second potential to the third potential, after controlled to the second potential.

Claim 16 (Original): The operation method according to claim 14, wherein the device has third and fourth bit lines which are arranged in a memory cell array different from a memory cell array in which the first and second bit lines are arranged, and an amplifier shared among the first and second bit lines and third and fourth bit lines, and the operation method further comprises,

electrically disconnecting the second bit line from the amplifier, and electrically connecting the fourth bit line to the amplifier after charges are transferred from one of the ferroelectric capacitor included in the first series connected TC unit type structure to the first bit line.

Claim 17 (New): The device according to claim 1, wherein the third potential is 0V.

Claim 18 (New): The operation method according to claim 14, wherein the third potential is 0V.